AMENDMENTS TO THE CLAIMS

The listing of claims replaces all prior versions, and listings, of claims in the application:

Listing of Claims

1-10. (Cancelled).

11. (New) A computer system clocking system, said system comprising:

at least two units with clock functionality, the units being coupled to a common system clock line, a common internal clock line, and a logic bus, wherein one unit is dedicated as a master unit at a time, the dedication of the master unit being dependent on at least a signal being given so as not to select a given unit for being a master unit, and if a given unit is dedicated as master unit when such a signal is given, the system performing a switchover causing another unit as the one not selected to be dedicated as master unit, each unit comprising:

a clock source for generating a clock source signal, the clock source signal being adapted for being output on the internal clock line; and

a phase lock loop device generating a signal, which is derived from the signal on the internal clock line, and which is output on the system clock line if the unit is dedicated as master unit, wherein one source clock signal of a unit is output on the internal clock line and all phase lock loop devices of all units generate phase lock loop output signals derived from the internal clock signal, the outputs of the phase lock loop devices being in phase with one another such that switchover from one phase lock loop output signal to another is seamless.

12. (New) The system according to claim 11, wherein the unit dedicated as master unit generates the clock source signal on the internal clock line.

13. (New) The system according to claim 11, wherein each unit further comprises:

a logic section communicating with the logic bus;

a first bi-directional port communicating with the internal clock line;

a second bi-directional port communicating with a system clock line, the logic section of the unit controlling the first and second bi-directional ports to input or output respective system clock signals and respective internal clock signals via enable signals.

14. (New) The system according to claim 13, wherein the enable signals first change state when the system clock is in a logic state with a certain predetermined security time interval from state changes of the system clock.

15. (New) The system according to claim 13, wherein the logic section, in cooperation with other logic sections of other units, negotiates a priority scheme according to which a predetermined order for dedicating units is determined.

16. (New) The system according to claim 11, wherein the logic section of any unit comprises fault sense circuitry and wherein, if a fault is detected in any device, the system initiates switchover from a dedicated unit to a subsequent dedicated unit.

17. (New) The system according to claim 11, comprising an additional board not comprising any clock generating or clock evaluating functionality, the additional board being coupled to the system clock line but not to the internal clock line nor to the logic bus.

18. (New) A computer system clocking unit comprising:

a logic section communicating with a logic bus;

a clock source for generating a clock source signal, the clock source signal being adapted for being output on an internal clock line;

a phase lock loop device having a predetermined characteristic and generating a signal, which is derived from a signal on an internal clock line;

first means for outputting the clock source signal to the internal clock line or inputting the internal clock signal from the internal clock line; and

second means for outputting the signal from the phase lock loop device to a system clock line or inputting the system clock signal;

wherein the logic section of the unit controls the first and second means to input or output respective system clock signals and respective internal clock signals and wherein, if the unit is dedicated as master unit, the logic section controls the phase lock loop generated signal derived from the internal clock signal to be output on the system clock line.

19. (New) The computer system clocking unit according to claim 18, wherein if the unit is dedicated as master unit, the logic section controls the source clock signal to be output on the internal clock line.

20. (New) The computer system clocking unit according to claim 18, wherein if the unit is not dedicated as master unit, the logic section controls the second means to input the system clock signal from the system clock line.

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